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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/955,874	09/18/2001	Mika Salmi	874.0100.U1(US)	9941

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EXAMINER
NGUYEN, LINH V

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 04/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/955,874	Applicant(s) SALMI ET AL.	
	Examin r Linh V Nguyen	Art Unit 2819	

-- The MAILING DATE of this communication appears on the cover she t with th correspondence address --

Period for R ply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2 – 9, and 11 – 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2 – 9, and 11 – 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

R sponse to Amendment

1. This office action is in response to applicant's amendment received on 04/01/03. Claims 1 and 10 have been canceled. Claims 2, 4, 5, 8, and 9 have been amended. Claims 17 – 21, have been added. Claims 2 – 9, and 11 – 21, are pending on this application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 2, 4, 5, 6, 8, 9, 11 and 13, are rejected under 35 U.S.C. 102(e) as being anticipated by Ichihara U.S. patent No. 6,249,560

Regarding to claim 2, Fig. 1 Ichihara et al. disclose a phase locked loop comprising a phase comparator (1) generating an output signal that is used to drive a voltage controlled oscillator (4), and a modulus prescaler (5,7,9,11) circuit coupled to an output of said voltage controlled oscillator (output), said prescaler circuit comprising an input node (input of 5) for coupling to said output of said voltage controlled oscillator for receiving an input signal having a characteristic frequency to be divided by L or N, an output node (a3) for outputting a frequency divided signal that is coupled to said phase

comparator (1), and a plurality of divider stages (5, 7) coupled between the input node and the output node for dividing the input signal by N and L, and further comprising at least one resampling stage (9) coupled to an output of at least one of said divider stages (7) for receiving an output signal therefrom and for synchronizing edges of the output signal to edges of the input signal (C Clock input of 9), thereby reducing temporal ambiguity in the occurrence of the edges of the output signal (improvement only no metes and bounds), where said at least one resampling stage is comprised of a flip-flop (9) having a data input coupled to said output of said at least one of said divider stages (7) and a clock input node (C of 9) for being clocked with said output of said voltage controlled oscillator (Fig. 1).

Regarding to claim 4, wherein said flip-flop is comprised of a D type flip-flop (9).

Regarding to claim 5, Fig. 1 Ichihara discloses a method of frequency source of a mobile station, comprising: operating a phase locked loop (Fig. 1) as part of the frequency source to generate a signal having a desired frequency (Output), the step of operating the phase locked loop including a step of dividing a frequency of an output signal of a voltage controlled oscillator (Output of 4) by a predetermined amount (N, L); to generated a frequency divided signal (a2, a1) and resampling (9) the frequency divided signal using a flip flop circuit (9) that has a data input coupled to said frequency divided signal and a clock input that (C of 9) is clocked with the output signal of the voltage controlled oscillator to reduce jitter in the frequency divided signal .

Regarding to claim 6, wherein the step of resampling operates a modulus prescaler circuit (5,7,9, and 11 of figure 1) that is coupled to the output of the voltage

controlled oscillator, the prescaler circuit comprising an input node (input of 5) for coupling to the output of the voltage controlled oscillator for receiving an input signal having a characteristic frequency to be divided by (N, L), an output node for outputting a frequency divided signal (a3) that is coupled to a phase comparator (1) of the phase locked loop, and a plurality of the frequency divider circuits (5, 7) coupled between the input node and the output node for dividing the input signal by N, L, where the step of resampling is accomplished in a resampling stage (9) coupled to an output of at least one of the frequency divider circuits (7) for receiving an output signal (a2) therefrom ,and for synchronizing edges of the output signal to edges of the input signal (clocked input C of D flip-flop), thereby reducing jitter of the output signal (advantages or improvement only not a subject matter).

Regarding to claim 8, wherein said flip-flop is comprised of a D type flip-flop (9).

Regarding to claim 9. Fig. 1 Ichihara discloses a method to operating a phase locked loop as part of the frequency source to generate a signal having a desired frequency (Output), comprising: operating a multi-modulus prescaler (5,7,9,11) function of the phase locked loop to divide a frequency of an output signal of an oscillator (4) by a predetermined amount (N,L) to generate a frequency-divided signal; and resampling the frequency divided signal (9) using a flip-flop circuit that has a data input coupled to the frequency divided signal and a clock input that is clocked with the output signal of the oscillator (C clock input of 9).

Regarding to claim 11 wherein the step of resampling operates a prescaler circuit (5,7,9,11) that is coupled to the output of the oscillator (4), the prescaler circuit

comprising an input node (input of 5) for coupling to the output of the oscillator (output) for receiving an input signal having a characteristic frequency to be divided by (L, N), an output node (Q) for outputting a frequency divided signal (a3) that is coupled to a phase comparator (1) of the phase locked loop (Fig.1), and a plurality of the frequency divider circuits (5, 7) coupled between the input node and the output node for dividing the input signal by N, L, where the step of resampling is accomplished in a resampling stage (9) coupled to an output of at least one of the frequency divider circuits for receiving an output signal therefrom and for synchronizing edges of the output signal to edges of the input signal (C clocked of D flip-flop 9), thereby equalizing the delay added in different modes of the multi-modulus prescaler function (advantages/improvement only, not a subject matter).

Regarding to claim 13, wherein said flip-flop is comprised of a D type flip-flop (9) that is clocked with the input signal of the oscillator (C clocked of D flip-flop 9).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3, 7, and 12, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ichihara., as applied to claims 2, 5 and 9 above.

Fig. 1 Ichihara disclose a PLL with prescaler function to produce a desired frequency signal as applied to claims 2, 5 and 9 above, comprising every aspect of applicant's claimed invention, except for wherein the value of N and L are programmable. However It would have been obvious to one having ordinary skill in the art at the time the invention was made to program N and L divided values, since it has been held that broadly providing a programmable or automatic means to replace manual activity which has accomplished the same result involves only routine skill in the art (In re Venner, 120 USPQ 192). Furthermore programmable frequency divider is a well know art and conventional for PLL circuit of Cok et al Fig.1 (34) as cited in previous office action (US4,573,023)

6. Claims 14 – 21, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ichihara., as applied to claim 9 above.

Regarding to claims 14 – 16, Ichihara's Fig. 1, as applied to claim 9 above disclose a PLL with prescaler function to produce a desired frequency signal as applied to claim 9 above, comprising every aspect of applicant's claimed invention, except for explicitly teach a mobile station using the PLL circuit. However, a mobile station is only the intended of use and well knows for transceiver system is using PLL circuit (Applicant's IDS cited arts (Rapeli US5991605, or Jorgensen US5889443)). Furthermore it has been held that a recitation with respect to the manner in which a claimed apparatus is intend to be employed does not differentiate the claimed apparatus from prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham, 2 USPQ2d 1647 (1987).*

Regarding to claim 17 - 21, Fig. 1, Ichihara as applied to claim 14 – 16, above disclose every aspect of applicant's claimed invention.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (703) 305-1934. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

LVN

April 15, 2003

Michael Tokar
Supervisory Patent Examiner
Technology Center 2800